IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Edwin Park
Art Unit: 2182
Serial No.: 09/975,364
Examiner: Justin R. Knapp
Filed: 10/11/01
Docket: TI-31696
For: UNIVERSAL INTERFACE SIMULATING MULTIPLE INTERFACE PROTOCOLS

APPELLANTS' BRIEF UNDER 37 C.F.R. §41.37

Comissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

The following Appeal Brief is respectfully submitted in connection with the above-identified application in response to the Final Rejection mailed April 4, 2006. Please charge all required fees, including any extension of time fees, to the deposit account of Texas Instruments Incorporated, Deposit Account No. 20-0668.

REAL PARTY IN INTEREST

The real party in interest is Texas Instruments Incorporated, to whom this application is assigned.

RELATED APPEALS AND INTERFERENCES

There are no related appeals or interferences known to the Applicant's legal representative.

STATUS OF THE CLAIMS

Claims 1, 2, 4-6, 8 and 9 are the subject of this appeal. Claims 1, 2, 4-6, 8 and 9 are rejected. Claims 3, 7 and 10-23 have been cancelled. This application was filed on October 11, 2001.

STATUS OF THE AMENDMENTS

The Appellants filed an amendment under 37 C.F.R. § 1.111 on June 20, 2005 in response to the Office Action dated March 21, 2005. The Appellants filed an amendment under 37 C.F.R. § 1.116 on September 26, 2005 in response to the Office Action dated August 30, 2005. The Appellants filed an amendment on June 9, 2006 in response to the Office Action dated April 4, 2006, with no amendments to the claims.

SUMMARY OF CLAIMED SUBJECT MATTER

Specification page 7, line 1 to page 9, line 2, provides a concise explanation of the invention defined in independent claim 1. In the preferred embodiment, the universal interface apparatus is able to support a number of 2-4 wire (line) devices using a software programmable block in which the control and data waveforms needed to support the protocols are all run time programmable. The UIA is able to support as illustrative example, protocols such as I2S, SSP, I2C, SPI, SBI, synthesizer programming, etc. Also, for SSP/PCM the UIA will not only support basic modes line 8 kHz voice, but will also support a variety of data sync waveforms, slots and data rates. The UIA will also allow the pads (interface pins) to change mode from one protocol to another at set up or run time to support the various needs of the application and customers. Optionally, multiplexers can also be used in order to allow the UIA to support multiple peripheral devices in a time multiplexed environment using the same interconnection pads.

FIGURE 1A shows an illustrative hardware environment, including telephone circuitry 150 wherein the universal interface apparatus 100 is located. The universal interface apparatus enables communications between a central processing unit (CPU) or digital signal processor (DSP) 152 (or other control hardware/software) and peripheral devices 156, 160. The apparatus 100 includes processing circuitry that may be co-located, integrated, or even one-and-the-same with the CPU 152. In this example, the apparatus 100 has a number of input/output (I/O) lines 155. Some of the lines are coupled to a jack 158, enabling connection of the apparatus 100 to an "off-board" peripheral device 160 located apart from the telephone circuitry 150. The device 160 may comprise a component such as a multimedia card (MMC), etc. Other of the lines 155 are coupled to an "on-board" peripheral device 156 that is located on the telephone circuit 150, and accordingly hard-wired to the apparatus 100. The device 156 may comprise a component such as a radio front-end IC. The apparatus 100 includes still other lines 162, for connection to other peripheral device(s) (not shown).

The universal interface apparatus of this invention may be embodied by various hardware components and interconnections, one example of which is shown by the

apparatus 100 of FIGURE 1B. The components of the universal serial interface apparatus 100 include a controller 104, memory 114, storage 120, clock 110 and optional multiplexer 112 ("mux"). If desired, the foregoing components may be provided together on the same circuit structure 102, such as an application-specific integrated circuit (ASIC). In this embodiment, the circuit 102 includes multiple pads 118 such as pins, connectors, ASIC pads, terminals, or other means to couple signal paths between the circuit 102 and off-circuit devices to which the apparatus 100 is providing an interface.

In one embodiment, the apparatus provides an interface between a main processor (not shown, e.g., CPU 152) and the off-circuit, "peripheral" device. For communications with the main processor, the controller 104 includes numerous I/O lines 130. The controller 104 communicates with the peripheral device via the memory 114, pads 118, and optionally the converter 122 and mux 112. In another embodiment, the controller 104 and main processor may be co-located or even provided by the same device. For instance, the controller 104 may perform one application program involving main processor duties, and another, concurrent application program involving operation of the interface 100.

The controller 104 serves to selectively reconfigure components such as the clock 110, and memory 114, to interface a general purpose processor with an off-circuit, communications device attached to the pads 118. Additionally, by utilizing techniques such as time multiplexing using mux 112, the controller 104 may further direct the apparatus 100 to concurrently interface with multiple off-circuit devices coupled to the pads.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Rejection under 35 U.S.C. § 102 (e) as being anticipated by U.S. Patent No. 6,973,658.

ARGUMENT

Rejection under 35 U.S.C. § 102 (e) over U.S. Patent No. 6,973,658.

Claims 1, 2, 4-6, 8, and 9

Claim 1 includes "... a multiplexer coupled between the memory and the plurality of interconnection pads wherein the universal interface device concurrently interfaces with the plurality of different peripheral devices using time multiplexing of the plurality of interconnection pads." The references of record do not show, teach, or suggest the above recited limitation of claim 1. U.S. Patent No. 6,973,658 does not disclose a multiplexer for time multiplexing coupled between the memory and the plurality of interconnection pads wherein the universal interface device concurrently interfaces with the plurality of different peripheral devices. U.S. Patent No. 6,973,658 does not have a time multiplexer coupled between the memory and the interconnection pads. The multiplexer disclosed in Claim 15 of U.S. Patent No. 6,973,658 is not referred to as a time multiplexer coupled between the memory and the interconnection pads. Nothing in U.S. Patent No. 6,973,658 suggests that the multiplexer is for time multiplexing.

CONCLUSION

For the foregoing reasons, Appellants respectfully submit that the Examiner's final rejection of Claims 1, 2, 4-6, 8 and 9 is improper, and it is respectfully requested that the Board of Patent Appeals and Interferences so find and reverse the Examiner's rejection.

Please charge any fees necessary in connection with the filing of this paper, including any necessary extension of time fees, to Deposit Account No. 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,

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CLAIMS APPENDIX

1. A universal interface device, comprising:

a controller;

a configuration database coupled to the controller, said configuration database having stored therein a plurality of different configuration protocols for supporting a plurality of different peripheral devices;

a plurality of interconnection pads;

a memory coupled to the interconnection pads and controller, the memory is programmable by the controller in order to support any of the different peripheral devices; and

a multiplexer coupled between the memory and the plurality of interconnection pads wherein the universal interface device concurrently interfaces with the plurality of different peripheral devices using time multiplexing of the plurality of interconnection pads.

2. A universal interface device as defined in claim 1, wherein the controller comprises a state machine.

4. A universal interface device as defined in claim 1, further comprising a programmable clock coupled to the memory or the configuration database.

5. A universal interface device as defined in claim 1, wherein the controller selects a configuration protocol from amongst the plurality of configuration protocols in the configuration database, and uses the selected configuration protocol to configure the memory in order to support the peripheral device from amongst the plurality that is coupled to the plurality of interconnection pads.

6. A universal interface device as defined in claim 2, wherein the state machine includes a programmable routing and mapping scheme that allows the state machine to communicate with more than one peripheral device that is coupled to the plurality of interconnection pads.

8. A universal interface as defined in claim 2, wherein the memory can be divided up by the state machine into two or more parts in order to support a peripheral device coupled to the interconnection pads that requires continuous transfer of data, the state machine switching between the two or more parts of the memory during data transfer to the peripheral device.

9. A universal interface as defined in claim 2, wherein the state machine sets a portion of the memory to provide a tri-state control if one or more of the plurality of interconnection pads have to function as both an input and an output.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.